16X16 SRAM

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6T Cell design

SRAM is used to store bits using interconnected inverter gates. Fig. 1 shows the schematic I used to create the 6T SRAM cell. The outputs of each inverter gate are connected to the inputs of the opposite one. Both interconnections are connected one side of an NMOS transistor. These transistors are used as access gates.

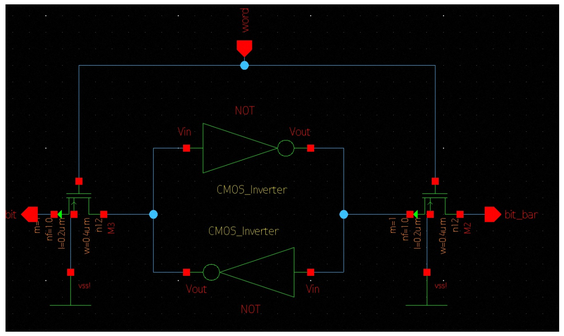

Fig. 1 6T Cell Schematic

Fig. 2 shows the transistors inside the inverter gates. D1 and D2 are the driver transistors, they pull to ground for a bit of 0. P1 and P2 are the pull-up transistors, they produce a high voltage when there is a bit 1 written to the cell. A1 and A2 are the access transistors. When a positive voltage is applied to the gates (word line) of the access transistors then the bit lines (bit or bit_bar) can either be written to or read from. If the word line is not positively charged, then the bit will be held.

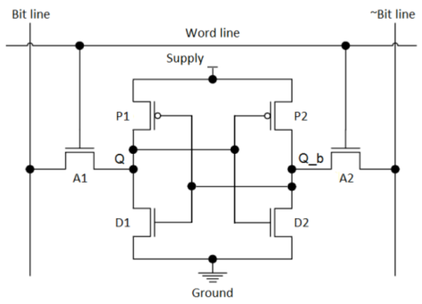

Fig. 2 6T Transistor Level Schematic

16x16 SRAM

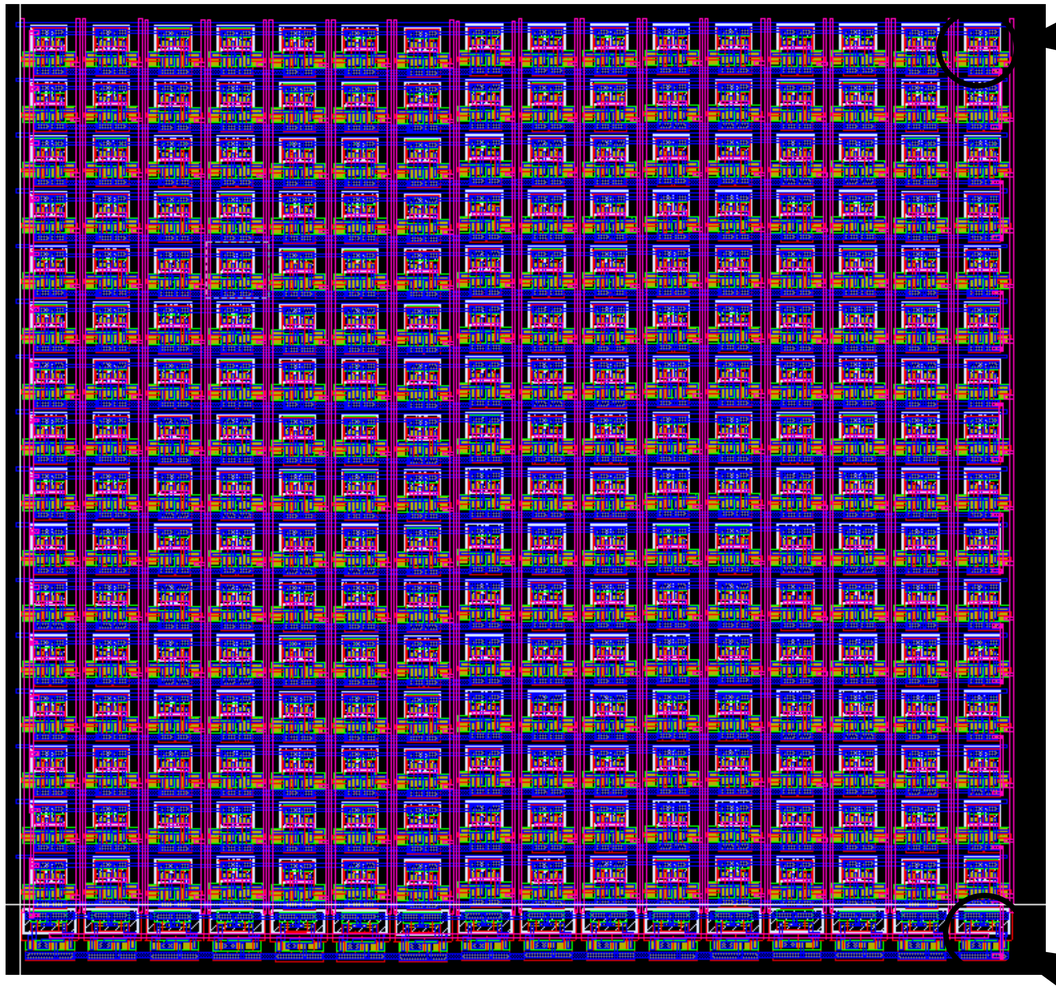

Fig. 3 16X16 SRAM Layout

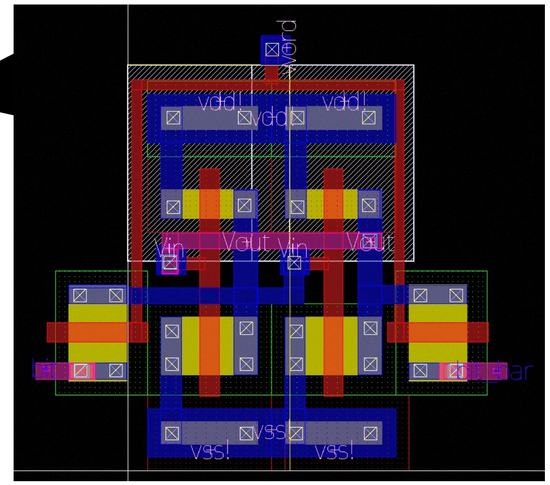

Fig. 4 6T Cell Layout

Fig. 3 shows the final layout of a 16X16 SRAM. This could hold 256 bits or 16 hexadecimal words. Fig. 4 shows the individual 6T cell layout. Each row is joined by word lines and each column is joined by bit and bit_bar lines. The sense amplifier connects to the bit and bit_bar lines and produce a positive voltage or a zero-voltage depending on the bit that is stored in the cell that is being read. Fig. 5 show s the layout of the sense amplifier.

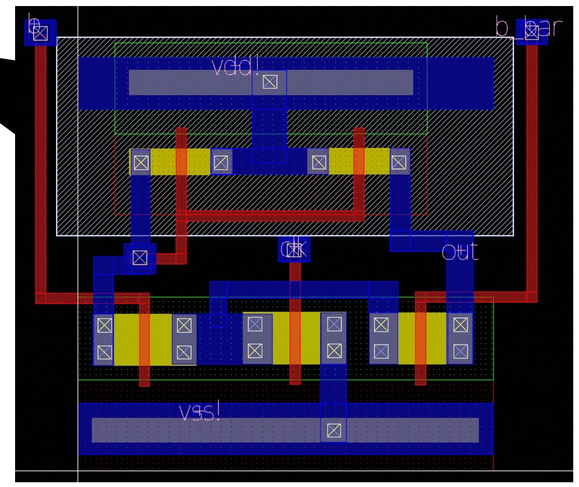

Fig. 5 Sense Amplifier Layout

REFERENCES

[1] Apostolidis, G., Balobas, D. and Konofaos, N., 2016. Design and Simulation of 6T SRAM Cell Architectures in 32nm Technology. [online] Jestr.org. Available at: <http://www.jestr.org/downloads/Volume9Issue5/fulltext23952016.pdf> [Accessed 9 November 2021]

[2] P. A. Mason, “Memory Basics.” [Online]. Available: https://www.egr.msu.edu/classes/ece410/mason/files/Ch13.pdf.