



Vending Machine

Trevor Ploederl, Brandon Leyde, Matthew Lueck
Faculty Mentor: Dr. Puteri Megat Hamari
ECET Department, Minnesota State University, Mankato



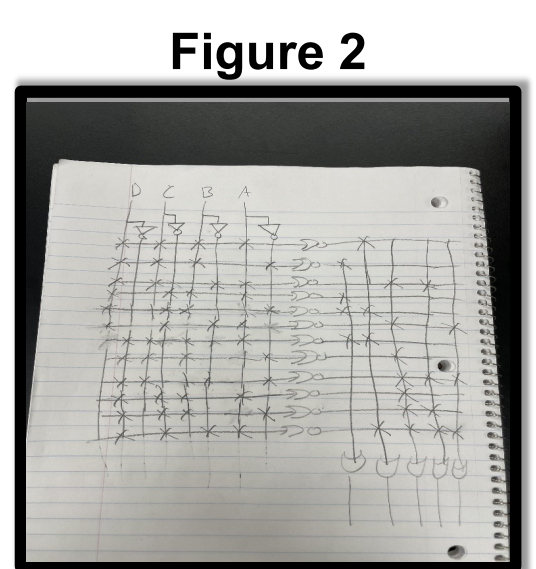
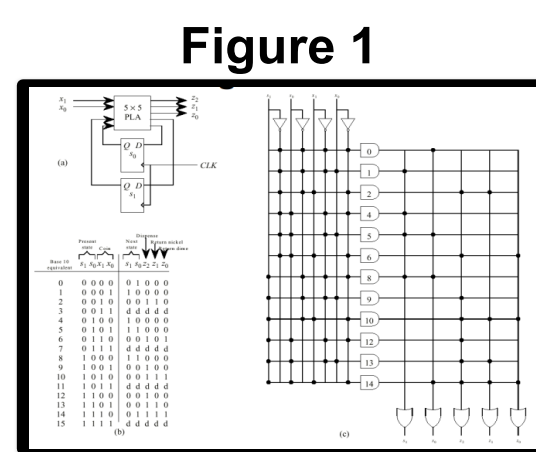
BACKGROUND

The original design

Design a finite state machine for a vending machine controller that accepts nickels (5 cents each), dimes (10 cents each), and quarters (25 cents each). When the value of the money inserted equals or exceeds twenty cents, the machine vends the item and returns change if any and waits for next transaction.

Room for improvement

We found an existing design for a vending machine that fulfills these functions, however we noticed we could further improve the design by doing AND to NOR gate conversions.

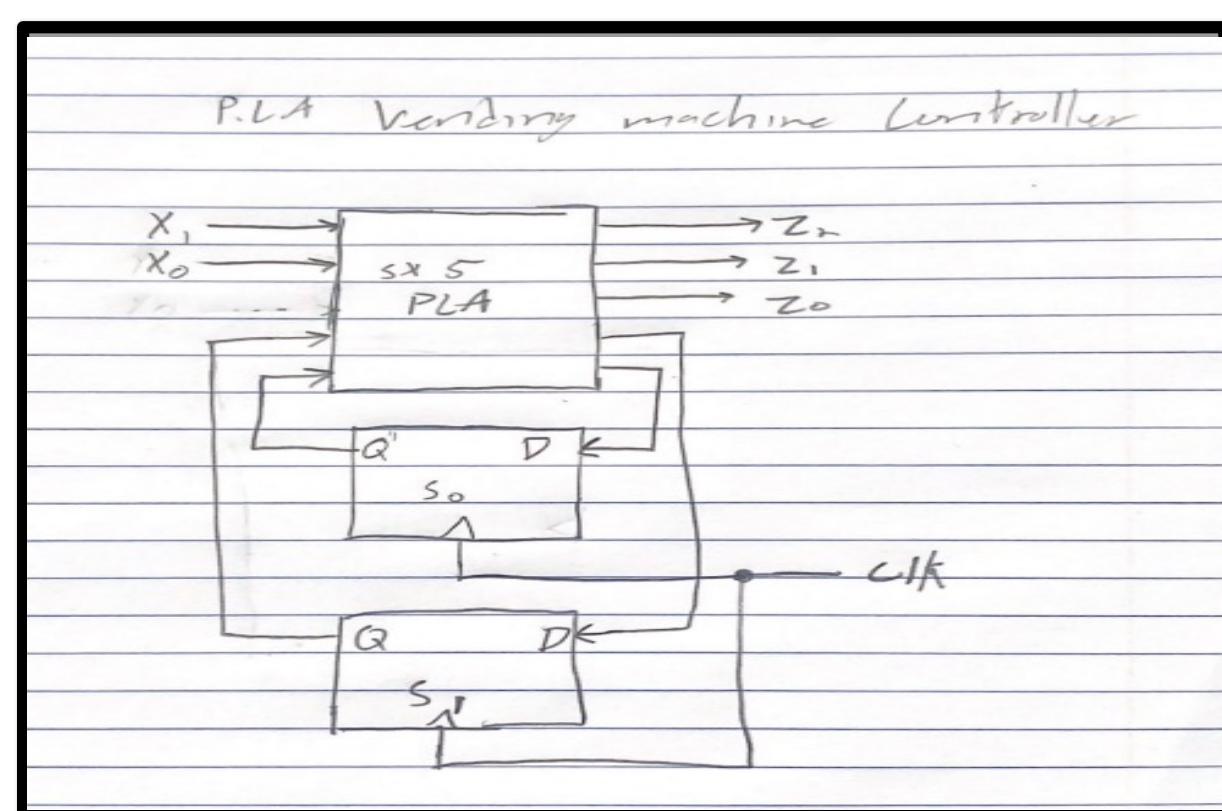


PROPOSED SOLUTION

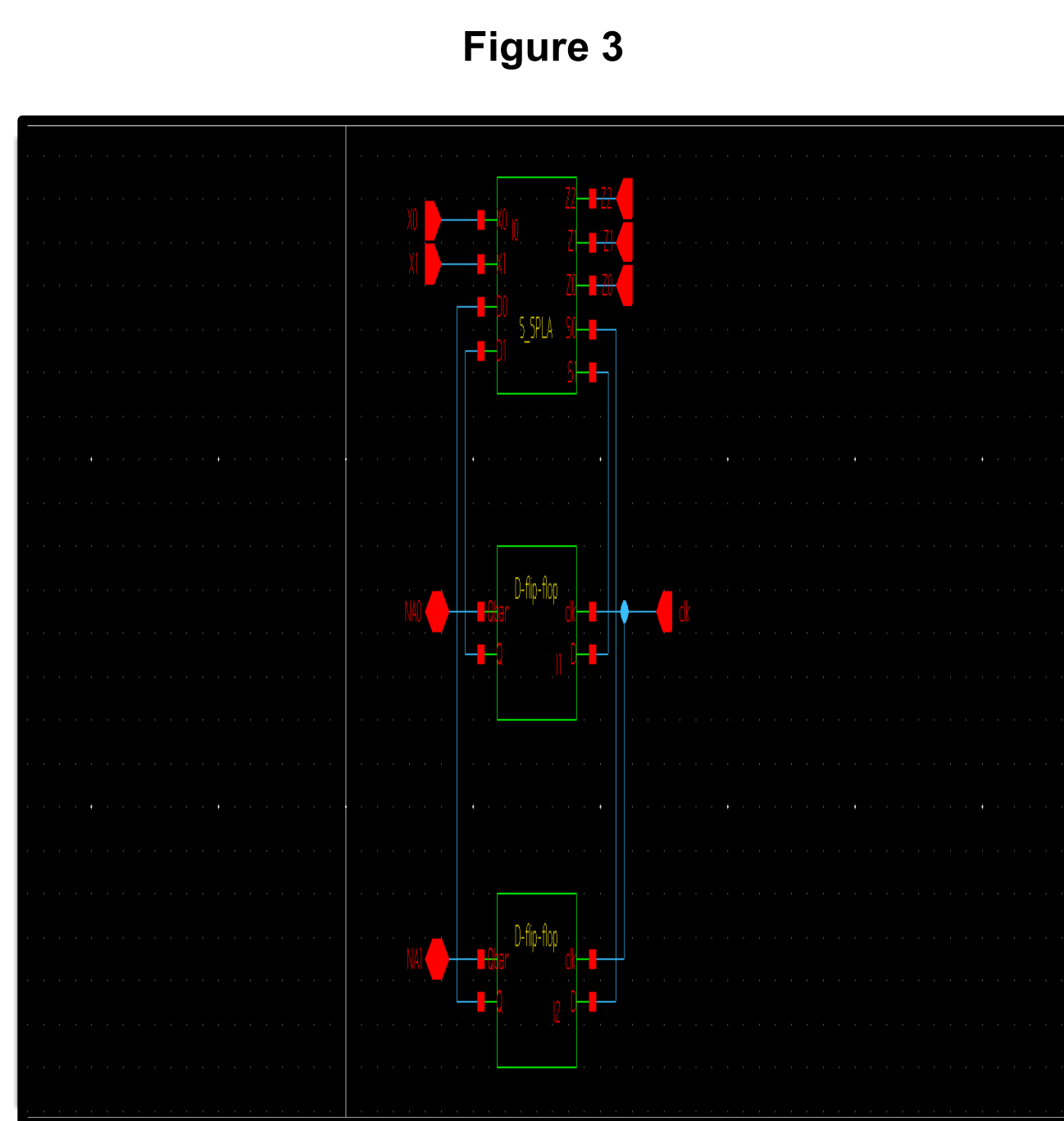
NOR and OR simplification

Our proposal is to design a vending machine and simplify it to use less transistors through the use of NOR gates instead of AND. Using the VLSI technical skills, we have practiced throughout the semester. We have redesigned a vending machine to be more efficient and dispense Hot Cheetos. If the user exceeds twenty cents the machine will dispense the user's change. So, once the value of the money inserted equals or exceeds the price of the hot Cheetos the vending machine will dispense the item, returns change if any, We tend to implement our design using a 4x5 PLA and two D flip-flops. Our vending machine will be a finite state machine. The example 5x5 PLA we looked at uses AND gates, but we decided to use 4 input NOR gates to reduce the number of transistors by 24. This will optimize our design, and which will reduce the delay and area of our total design. The finished out of a design of 98.5µm

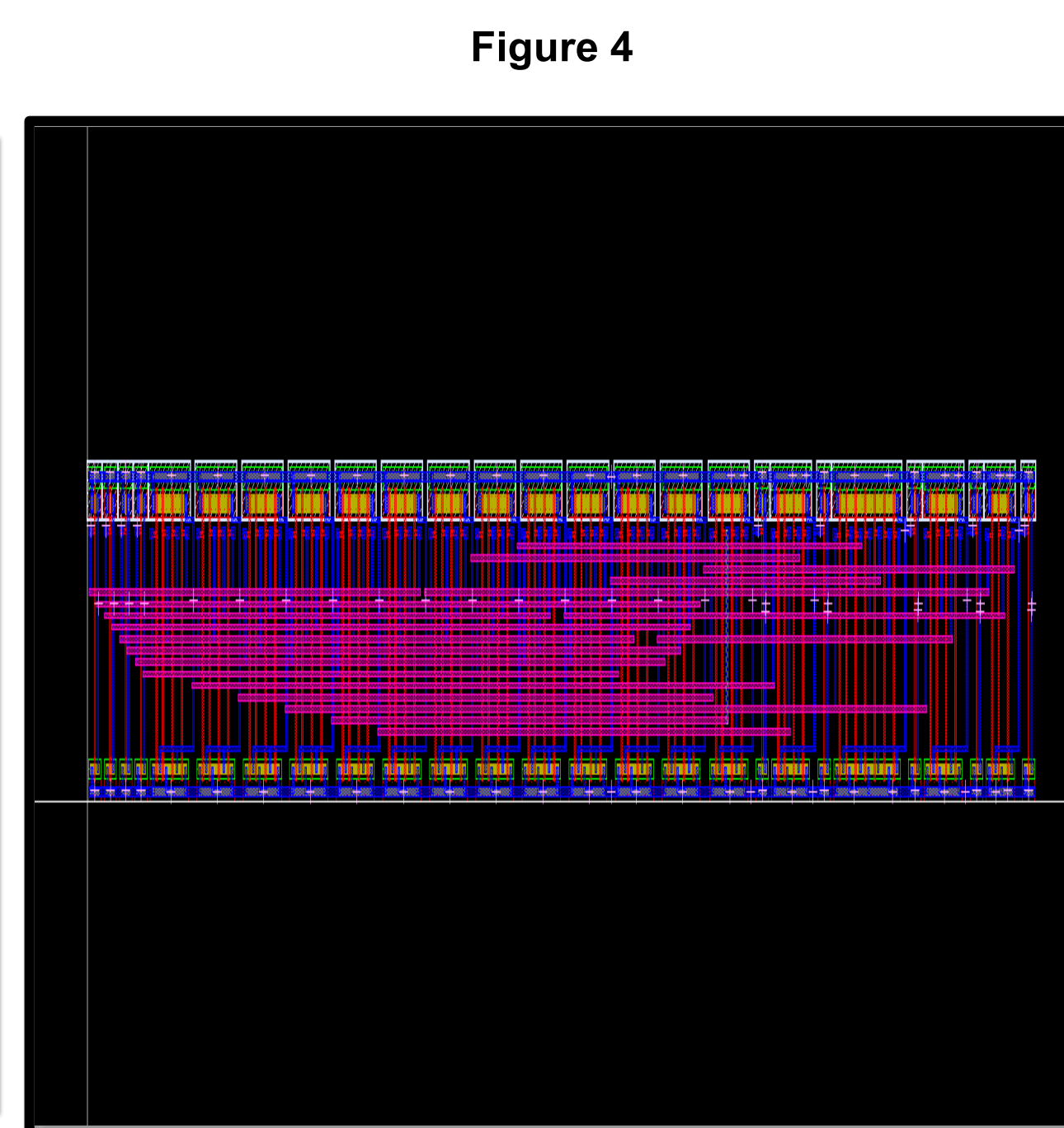
Figure 3



SYSTEM DESIGN



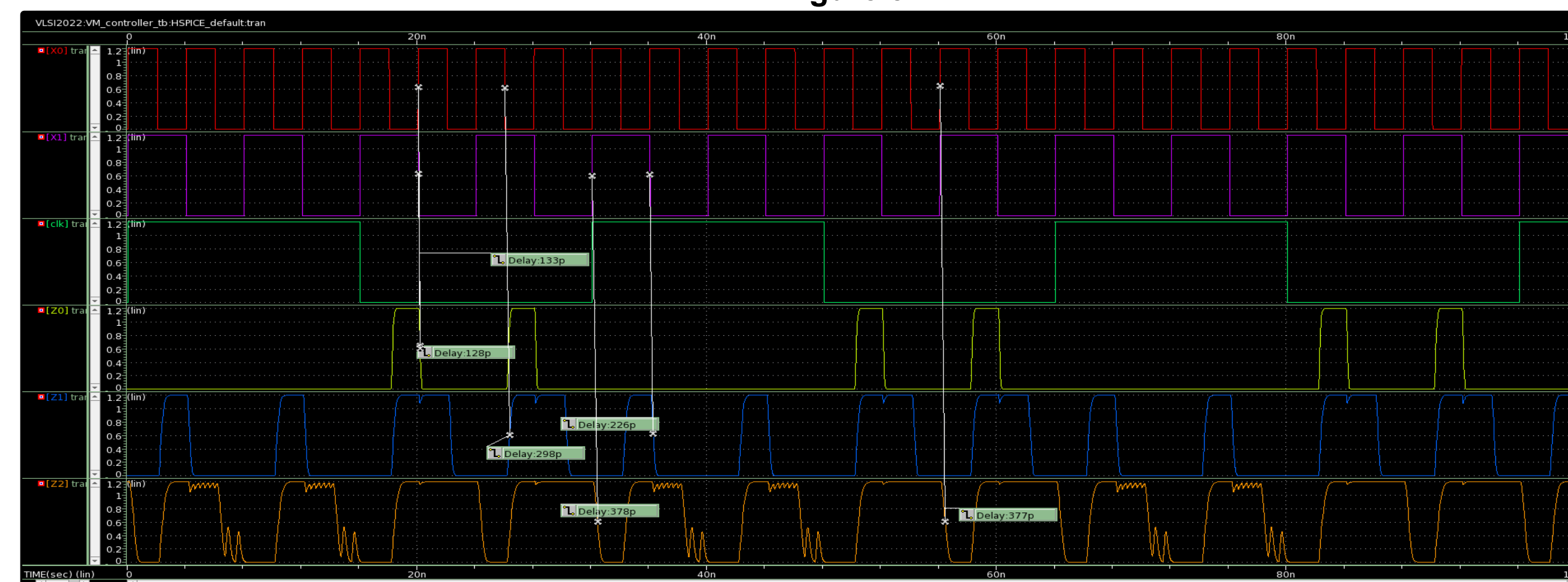
Vending Machine Schematic



Vending Machine Layout

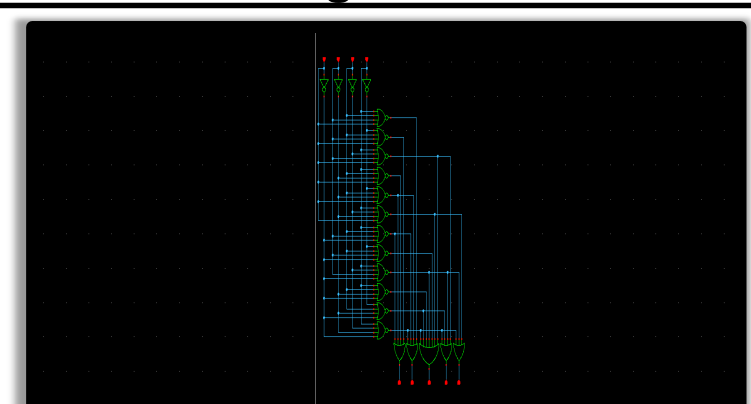
Results

Figure 5



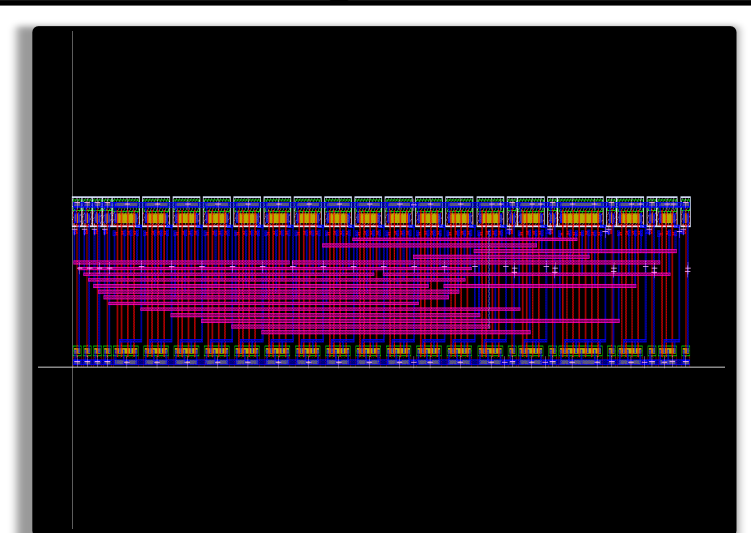
Vending Machine Controller Waveform

Figure 6



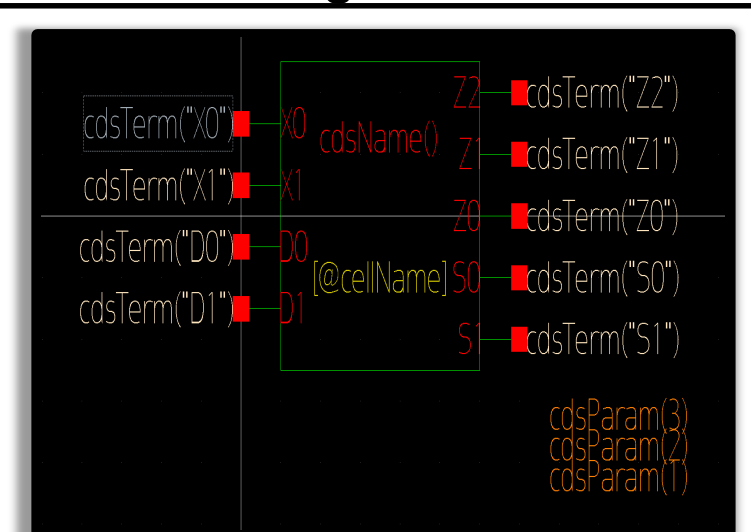
5x5 PLA Schematic
The PLA uses 4 inverters, 11 4 input NOR's, 3 4 input OR's 1 7 input OR and a 3 input OR.

Figure 7



5x5 PLA Layout
The layout of the PLA has a width of 75µm

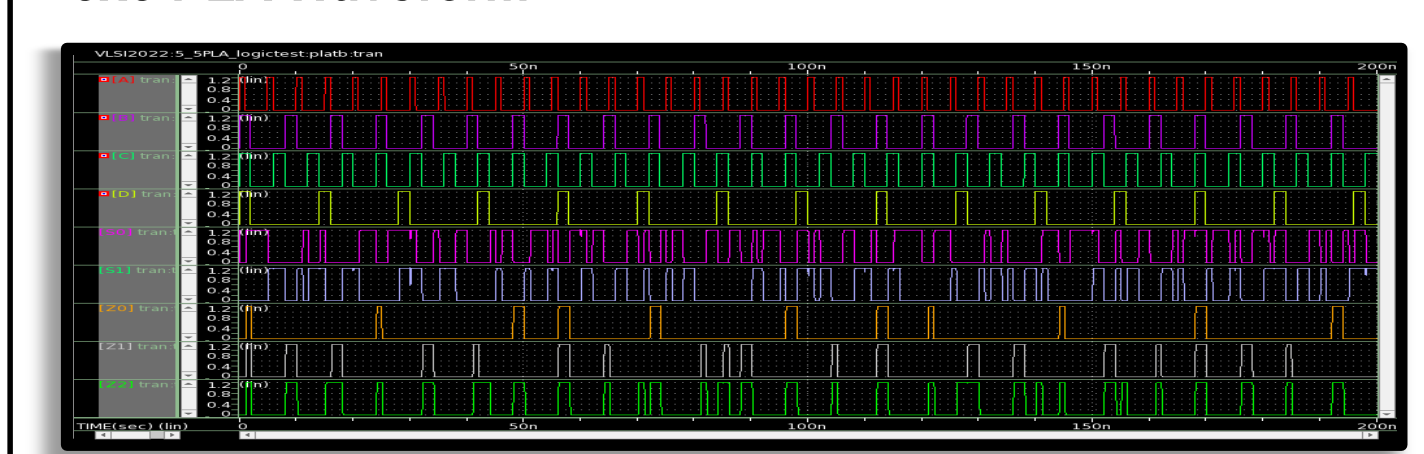
Figure 8



5x5 PLA Symbol
The symbol makes it easier for the test bench schematic that shows the waveform below.

Figure 9

5x5 PLA Waveform



ACKNOWLEDGEMENTS

We would like to thank Dr. Puteri Megat Hamari for being our mentor during this Design project.

REFERENCES

UMBC CMSC 313 Digital Logic Slides, <https://redirect.cs.umbc.edu/courses/undergraduate/CMSC313/fall06/burt/slides/>.

CONTACT INFORMATION

Feel free to contact us at Brandon.leyde@mnsu.edu, Trevor.ploederl@mnsu.edu and Matthew.lueck@mnsu.edu with any questions or comments.