Fast Binary Counters

Caleb Percy

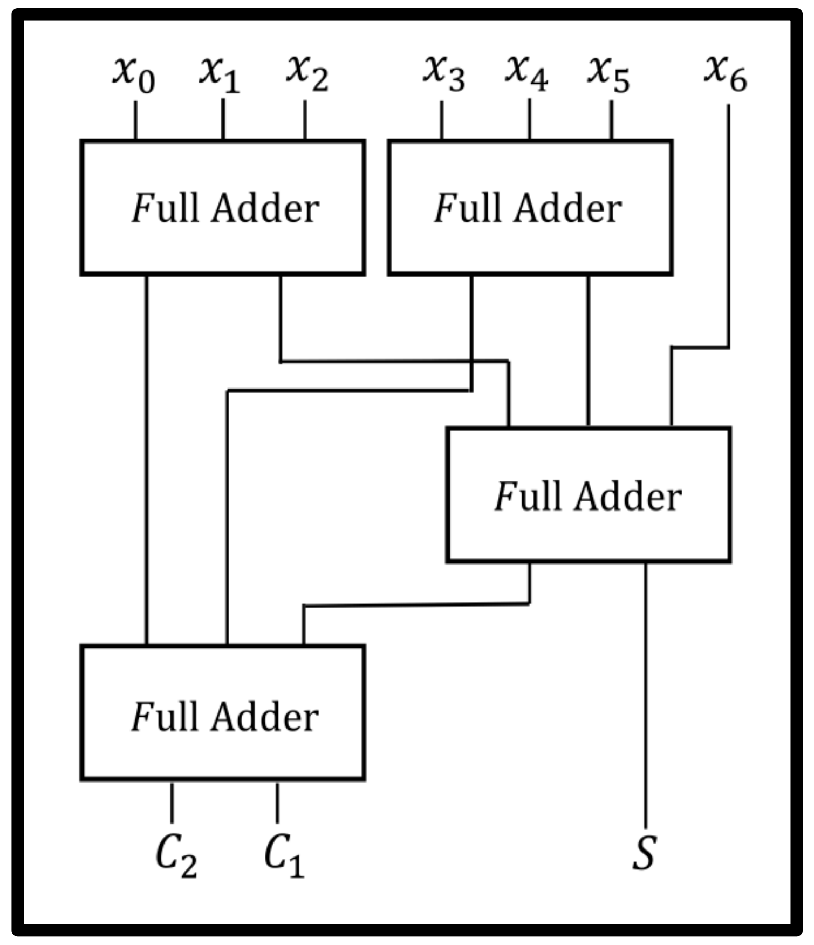
Faculty Mentor: Dr. Puteri Megat Hamari

ECET Department, Minnesota State University, Mankato

BACKGROUND

The summation of multiple operands is used all over the industry. Usually a basic multiplier circuit adds up the partial products by using full adders, also known as the Wallace Tree structure(Figure 1). This structure uses these adders as (3,2) counters in order to accelerate the summation. This method is often also referred to as the carry-save structure as well. However every time an adder is put into the circuit time goes up logarithmically. Since then papers have been trying to find more time effective strategies to accomplish this same idea.

Figure 1



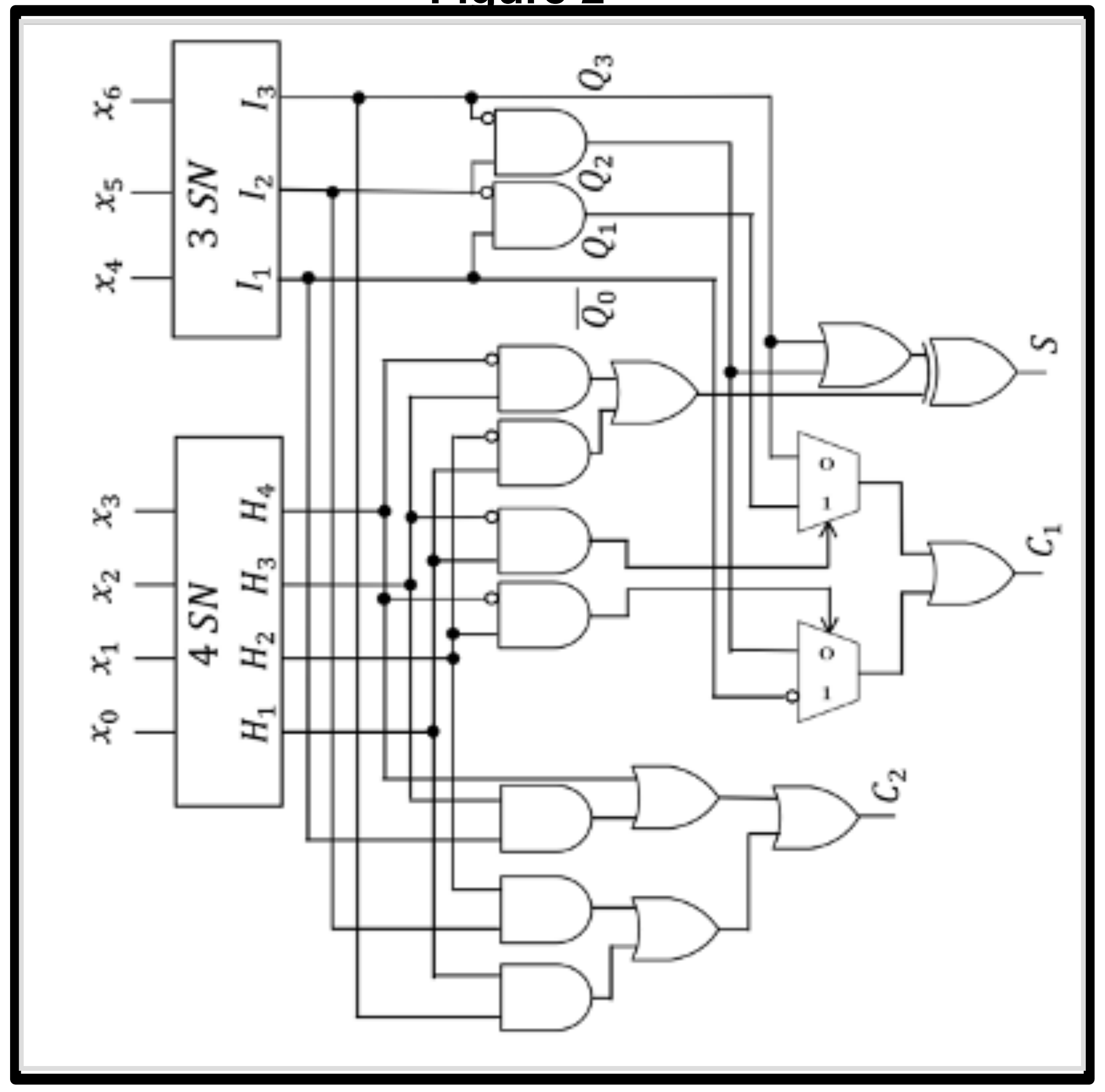
The Idea:

One of the bigger ideas out in the industry is to construct a compressor with a higher compression ratio than (3,2) by adding more bits at the same weight. Papers have discussed a whole slew of different input ratios that could improve timing. (4,3), (5,3), (6,3), and (7,3) input ratios have all been discussed in papers.

PROPOSED SOLUTION

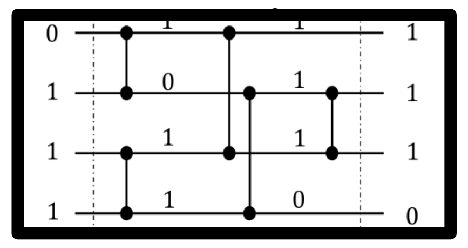
Instead of using the traditional adders two sorting networks are implemented asymmetrically. This circuit(Figure 2, Figure 3)now implements three different Boolean expression making for largely simplified outputs and proving to have 8.1%-27% less delay, taking up less area, and consuming less power.

Figure 2



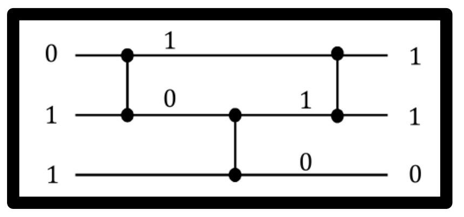
SYSTEM DESIGN

4 input Sorter



The 4 input sorter acts as a buffer for the top four inputs. It takes whatever input is coming in and sorts them from least to greatest. In this case it drives all of the ones to the top(x0) and the zeroes to the bottom(x4).

3 input Sorter



The 3 input sorter acts as a buffer for the bottom 3 inputs. It takes whatever input is coming in and sorts them from least to greatest. In this case it drives all of the ones to the top(x5) and the zeroes to the bottom(x7).

S

Serves as the 1 place in outputting the number. With all sorters working S should output 1 if an odd number of inputs are turned on and if an even number of inputs are on it will output 0

$S = (P1|P3) \oplus (Q1|Q3)$

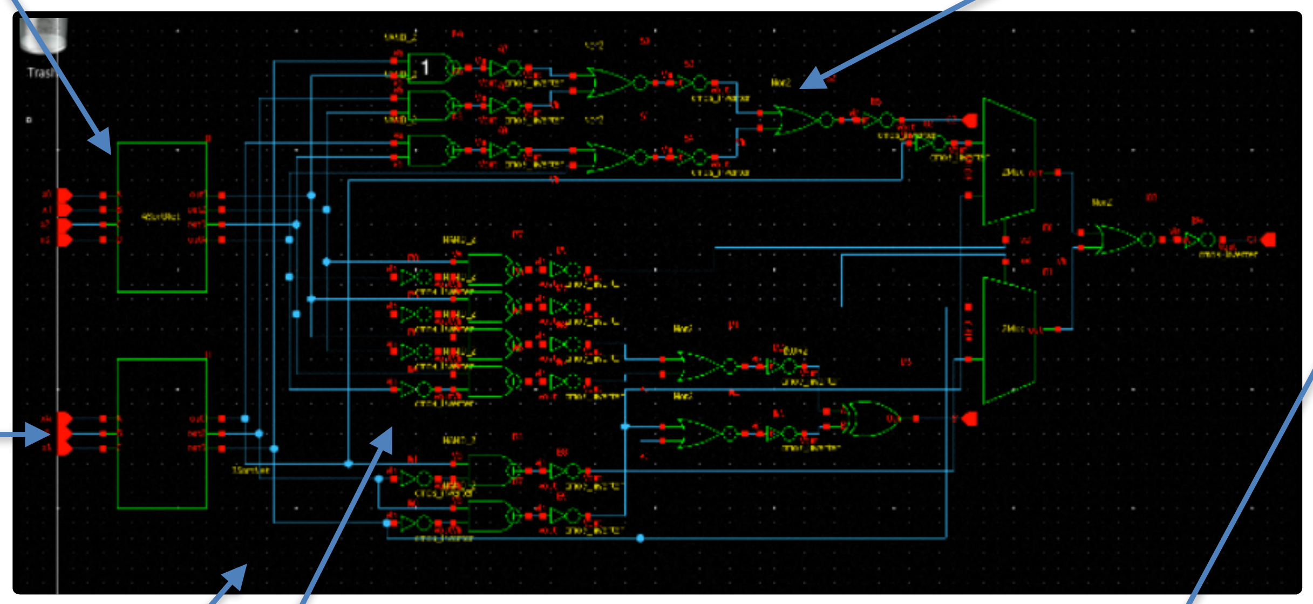
C1

Serves as the 2 place in outputting the number. With all sorters working C1 should alternate between 1 and 0 every time the inputs are change by a factor of 2.

$C1 = (Q0\&(P2|P3))|(Q1\&(P1|P2))|$

$(Q2\&(P0|P1)|P4))|(Q3\&(P0|P3)|P4))$

Figure 3



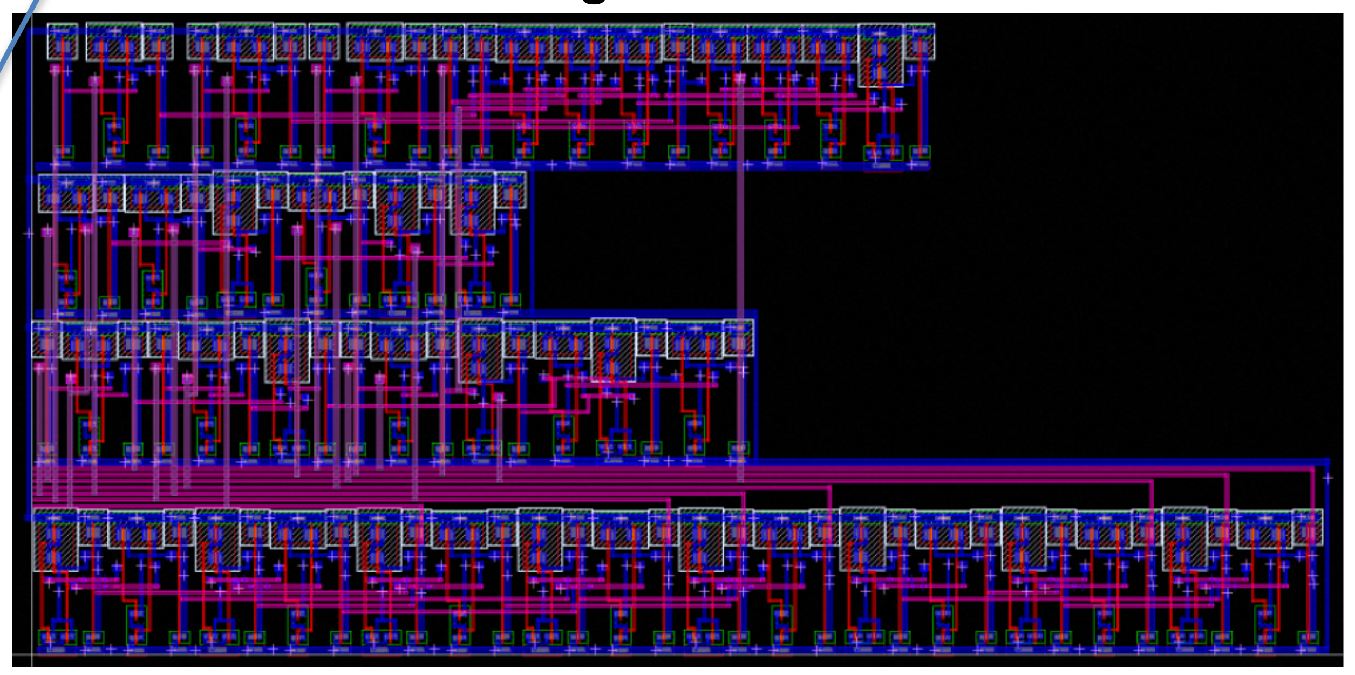
Final Circuit

C2

Serves as the 4 place in outputting the number. With all sorters working C2 should alternate between 1 if the amount of inputs turned on is greater than or equal to 4. Otherwise C2 should output 0.

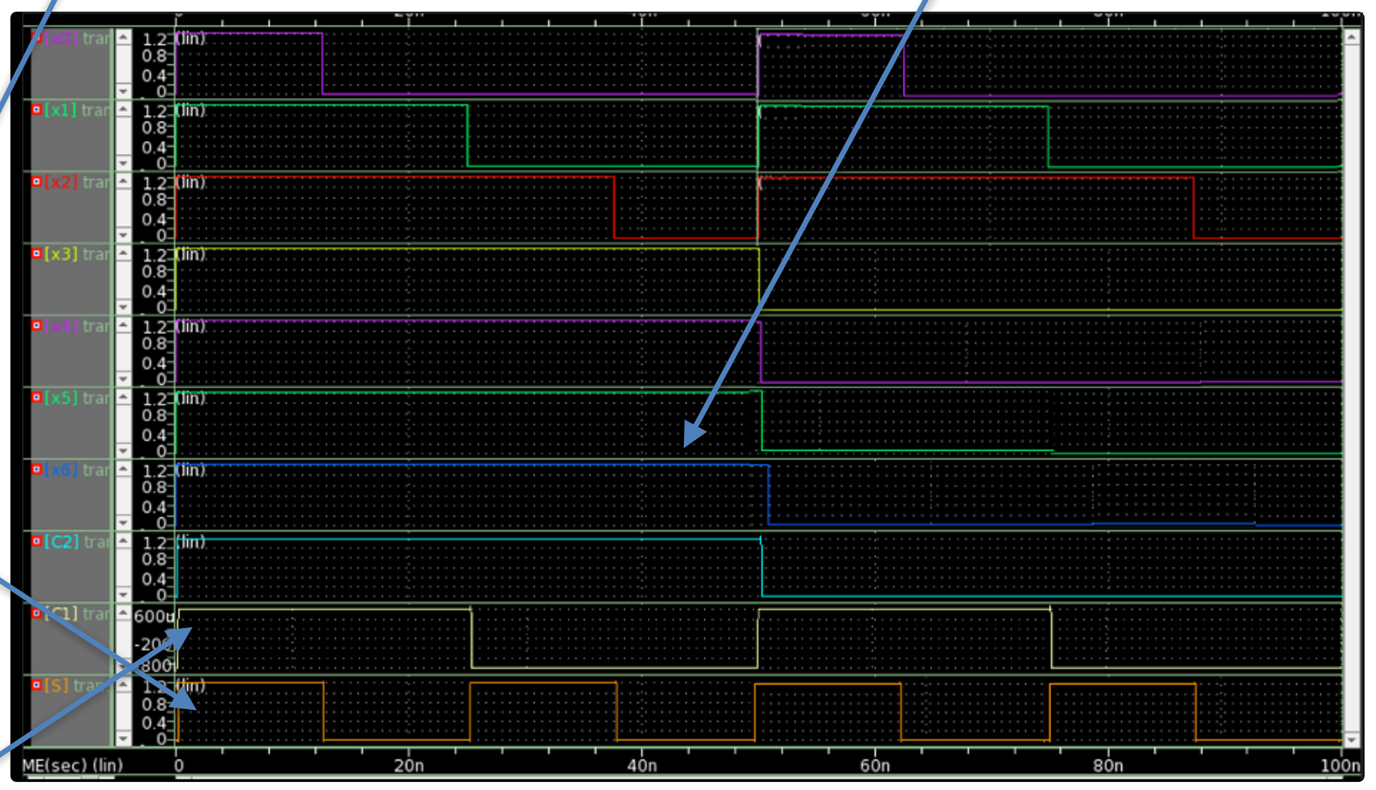
$C2 = P4|(P3\&Q0')|P2\&(Q2|Q3)|(P1\&P3)$

Figure 4



Final Layout

Figure 4



Final Waveform

input	C2	C1	S
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

FUTURE DIRECTION

- Expand the amount of inputs from (7,3) to (15,4) and even (31,5)
- Construct bigger more well connected sorting networks to allow more inputs
- Create and refine other binary equations to allow for a fourth bit
- Simplify circuit even further by putting half-sorting networks in places in the middle of the circuit.

ACKNOWLEDGEMENTS

I would like to thank Dr. Megat Hamari for teaching a really challenging but fun and interesting class and helping me through my many mistakes and troubles along the way.

REFERENCES

[1] W. Guo, S. Li. Fast Binary Counters and Compressors Generated by Sorting Network. 2021.

CONTACT INFORMATION

Feel free to contact me at caleb.percy@mnsu.edu