Synchronous Counter

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BACKGROUND

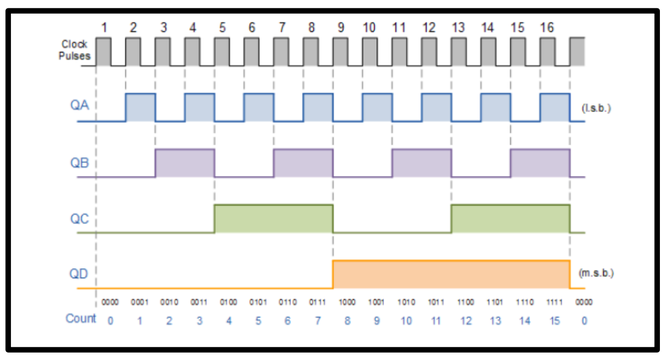
A counter is a device which can count any particular event on the basis of how many times the particular event(s) has occurred. In a digital logic system or computers, this counter can count and store the number of times any particular event or process have occurred, depending on a clock signal. The outputs represent binary or binary coded decimal numbers. Each clock pulse either increase the number or decrease the number.

Synchronous means that something is coordinated with others based on time. Synchronous signals occur at the same clock rate and all the clocks follow the same reference clock. In synchronous counters, the clock input across all the JK flip-flops use the same source and create the same clock signal at the same time.

Operation

The 4-bit Synchronous up counter start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then starts a new counting cycle by getting reset. There is no propagation delay in the synchronous counter due to all of the JK flip-flops in parallel with the clock source and the clock triggers all counters at the same time.

Waveform Timing



SYSTEM DESIGN

In the first clock pulse, the outputs of all the flip flops will be 0000. In the second clock pulse, as inputs of J and K are connected to the logic HIGH, outputs of JK flip flop(FF0) changes. This results in the output of the first flip-flop(FF0) to changes its state for every clock pulse. In the third clock pulse next flip flop (FF1) will receive its J, K inputs and changes its state. At this time, (FF0) will change its state to 0. And thus, input on the (FF1) is 0. Hence output is -0010. Similarly, in the fourth clock pulse (FF1) will not change its state as its inputs are in LOW state, it remains in its previous state. Though it produces the output to (FF2), it will not change its state due to the presence of the AND gate. (FF0) will again toggle its output to logic HIGH state, outputting 0011. Lastly, in the fifth clock pulse, (FF2) receives the inputs and changes its state. While (FF0) will have LOW logic on its output and (FF1) will also be in LOW state producing 0100. This process continues up till output 1111.

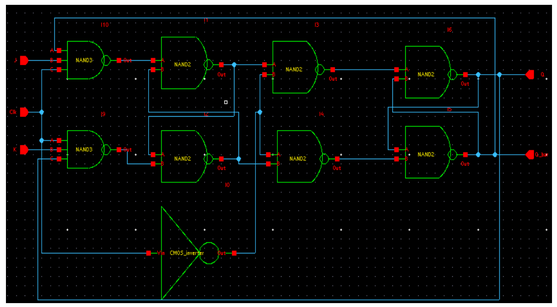


Figure 1. JK Flip-Flop Schematic

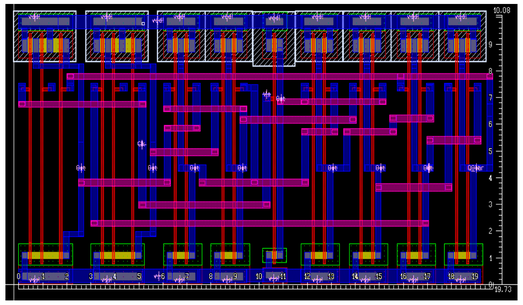


Figure 2. JK Flip-Flop Layout

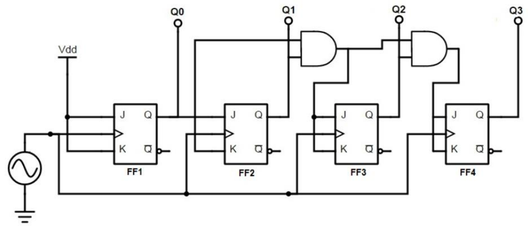


Figure 3. Synchronous Counter Schematic

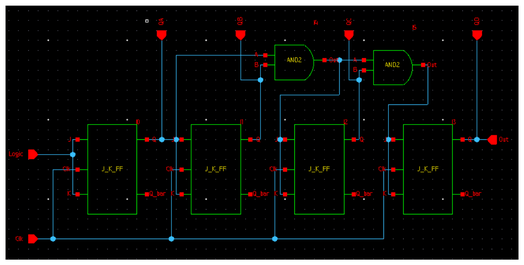


Figure 4. Synchronous Counter Schematic

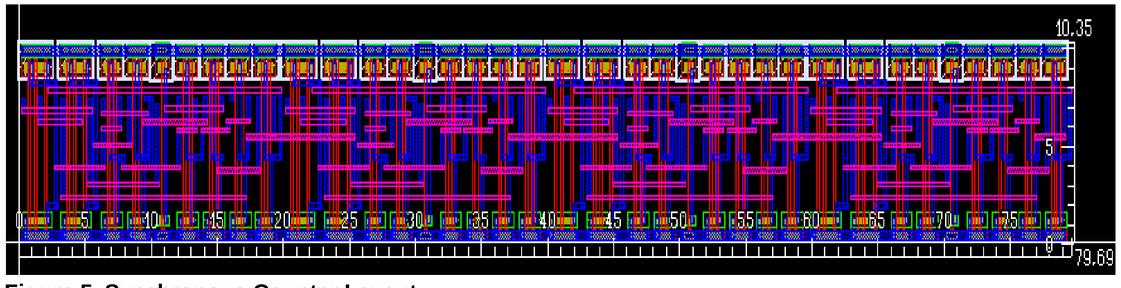
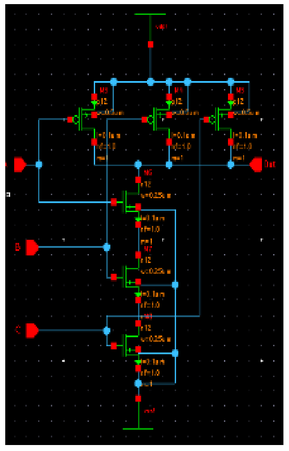


Figure 5. Synchronous Counter Layout

Operation Table

Clock pulse	Q4	Q3	Q2	Q1	Output	Output
1st Clock Pulse	Low	Low	Low	Low	0	0
2nd Clock Pulse	Low	Low	Low	High (starts toggling)	1	1
3rd Clock Pulse	Low	Low	High	Low	2	10
4th Clock Pulse	Low	Low (AND condition is not satisfied)	High (Remembers)	High	3	11
5th Clock Pulse	Low	High	Low (toggles)	Low	4	100
6th Clock Pulse	Low (AND condition not satisfied)	High (Remembers)	Low (remembers)	High	5	101
7th Clock Pulse	Low (AND condition satified)	High	High	Low	6	110
8th Clock Pulse	Low	High	High	High	7	111
9th Clock Pulse	High	Low	Low	Low	8	1000
10th Clock Pulse	High(Remembers)	Low	Low	High	9	1001
11th Clock Pulse	High	Low	High	Low	10	1010
12th Clock Pulse	High	Low	High	High	11	1011
13th Clock Pulse	High	High	Low	Low	12	1100
14th Clock Pulse	High	High	Low	High	13	1101
15th Clock Pulse	High	High	High	Low	14	1110
16th Clock Pulse	High	High	High	High	15	1111



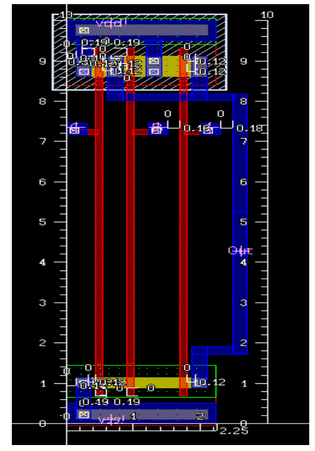


Figure 6. NAND3 Schematic

Figure 7. NAND3 Layout

ACKNOWLEDGEMENTS

I would like to thank Dr. Puteri Megat Hamari for teaching us VLSI.

REFERENCES

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2. https://www.electronicshub.org/synchronous-counter/#:~:text=4%20bit%20Synchronous%20DOWN%20Counter,-Down%20counter%20counts&text=This%20is%20similar%20to%20an,to%20all%20the%20flip%20flops.
3. https://www.electronics-tutorials.ws/counter/count_3.html

CONTACT INFORMATION

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