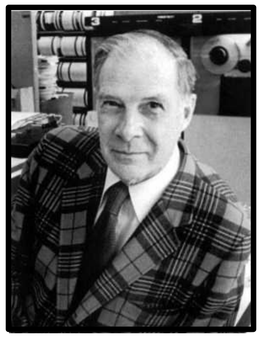
# (13, 8) Hamming Decoder

Colin Roskos, B.S. Computer Engineering

Minnesota State University Mankato

## BACKGROUND

In digital signal processing where the signal power is similar or near to the noise power, then a signal can become corrupted. When working over interplanetary distances the attenuation forces this case. Because of this there is the greater possibility of error in transmission. When using a digital method, there is an algorithmic method of correcting for this error. In the 1950s and 60s there was an emerging need to recover data from corrupted data. The methods that can be used for this application are called error-correcting codes. These codes are used to correct corrupted data back into their original intended form. Hamming Codes are a special type of error-correcting code in the family of linear error-correcting codes that relies on a set of overlapping parity checks which can recover data perfectly within a Hamming distance number of errors, where a block length n = 2r – 1 contains a message of length k = 2r – r -1. These codes are capable of a correction of Hamming distance – 2 and error detection of their Hamming distance - 1. This method of error correction is found where error rates are low and message sizes are kept to smaller lengths. This makes this widely used in EEC memory, and used in early space communications before the use of statistical processing.



**Richard Hamming**

## Project Idea

The project presented is a modified Hamming(15,11) with error detection decoder where only 8 data bits are used and an error detection bit has been added, giving a 13-bit word length in total.

This block has a 13-bit shift register with parallel select. With an output of an 8-bit corrected word with an error detection bit.

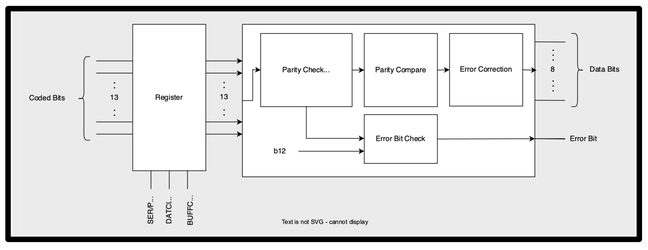



**Figure 1**

(Image Credit: CIO)

## SYSTEM DESIGN

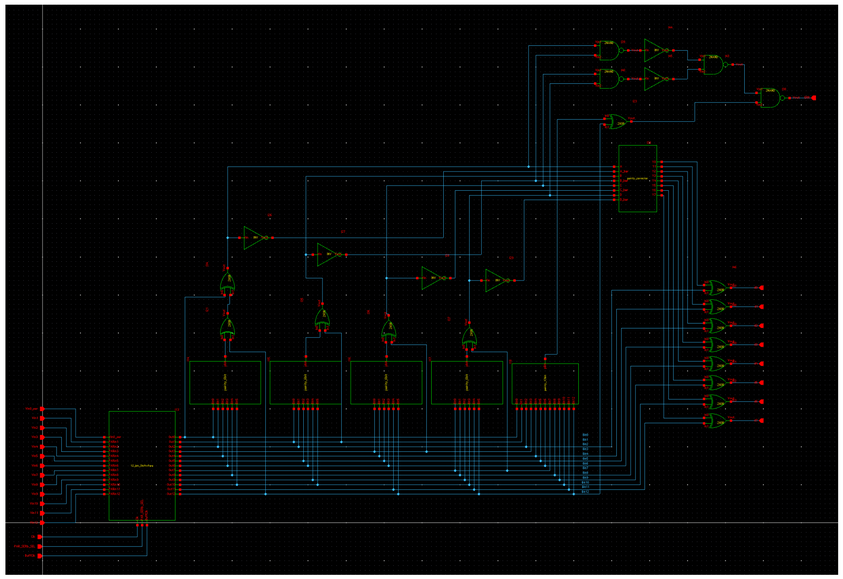


**Figure 2**

## Shift Register with Buffer

This shift register uses a inverting clock signal input, then uses a 2-bit MUX to determine the use of a serial clock or a parallel clock and serial or parallel input bit. The buffer will select the current state of the register by a buffer clock signal and will then use this as an input into the hamming decoder.

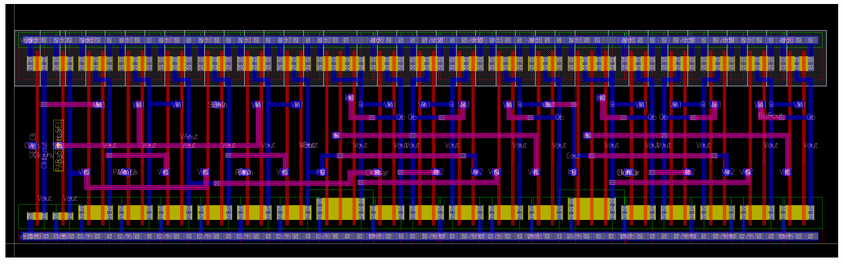


**Figure 3**

## Parity (6-bit, 7-bit and 13-bit)

The parity system is to calculate the received parity in each of the four parity bits as well as the error detection bit. This was done by XOR calculations between the input bits described in figure [].

## Correction Decoder

The correction decoder was created by modifying a standard 8-bit decoder to use four input bits, the calculated parity bits, Then this output is XORed with the received input bits, b2, b4, b5, b6, b8, b9, b10, b11.

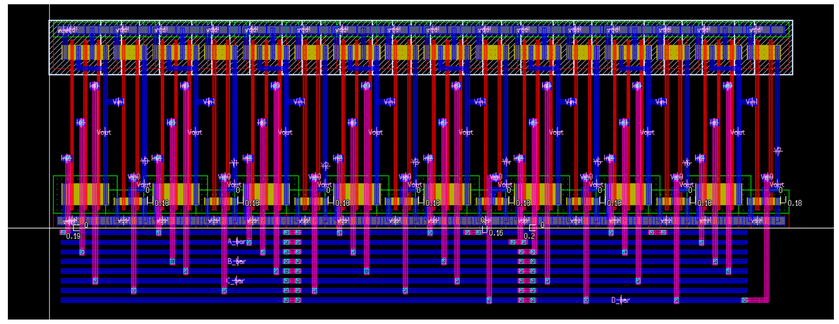


**Figure 4**

## Error Detection

If a correction is made (decoder has a non-0 output), and the Error bit shows no error, an error is detected. If there is no correction, but the error parity bit shows an error then there is an error. Only one error can be corrected, and two errors detected.

## ACKNOWLEDGEMENTS

We would like to thank Dr. Hamari for supporting this project as well as the VLSI Design professor.

## CONTACT INFORMATION

Feel free to contact us at colin.roskos@mnsu.edu with any questions or comments.