Sequential & Dynamic 4-bit Comparator

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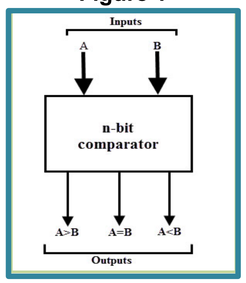
BACKGROUND

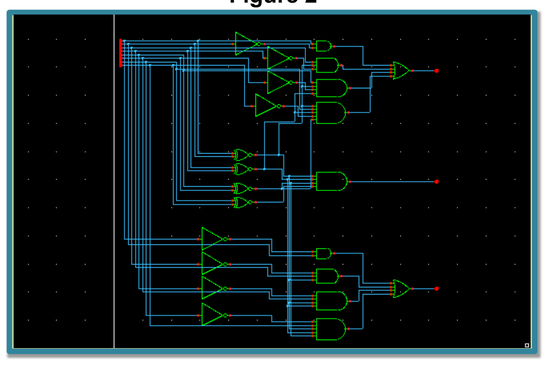
The ideal function of a comparator is to take two binary stringed inputs, compare the strength, and output whether the second string greater than, less than, or equal to the first binary string. The idea of logic here is relatively simple but requires many gates to achieve the result. There are many ways to accomplish this goal, but within this project we aim to compare the most fundamental designs.

Figure 1



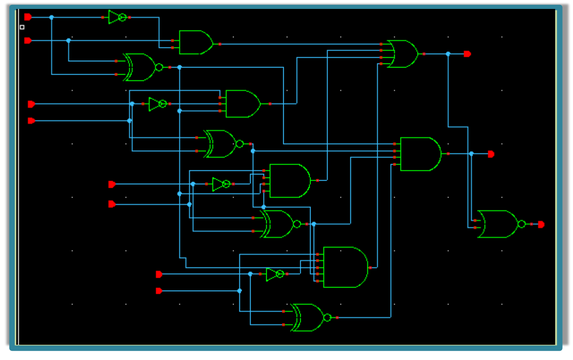
Dynamic Design aims to create the proposed solution in an instantaneous fashion. Thus, computing all the logic at once, or in this case in three separate blocks (one for each output). The schematic of the proposed solution is shown in *Figure 2.*

Figure 2



Sequential Design takes a similar but opposite approach to accomplishing the problem. Instead of computing all the logic straight at once, we instead use denoted states to discover the answer either with less delay or less area taken. The states approached are shown below in *Figure 4* and the proposed reduced form of the circuit is shown in *Figure 3.*

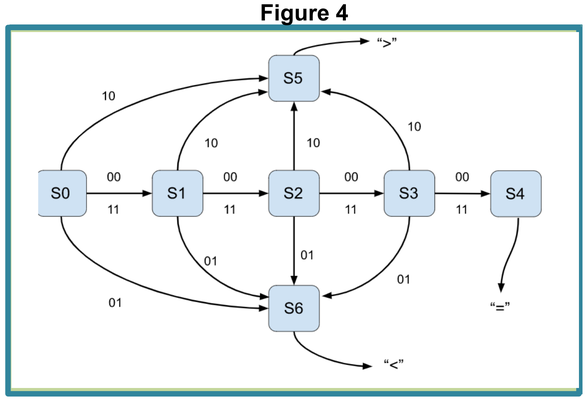
Figure 3



SYSTEM DESIGN

As you can observe through the dynamic layout (*Figure 5)* and the sequential layout (*Figure 6)*, the space and shape of each is drastically different. Within the dynamic the input logic is sent along transmission lines that deliver the signal to different blocks of the circuit. The sequential instead uses the logic embedded within one long trace that is considered in steps. The path traveled in the sequential appears longer than any of those seen in *Figure 5* hence it follows that the produced delay is slightly greater. Due to simplicity however the structure of *Figure 6* is much more convenient for implementation in tight circuits such as CPUs. Each system was built with minimum area as well as the least amount of trace levels needed.

Figure 4



State Diagram

Figure 5

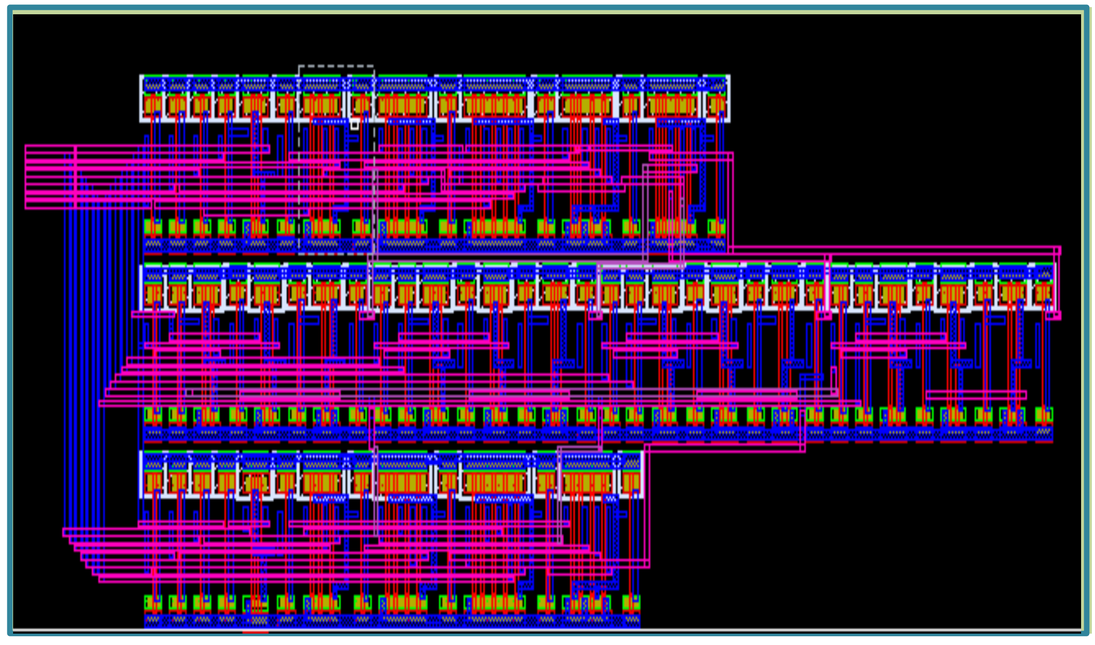
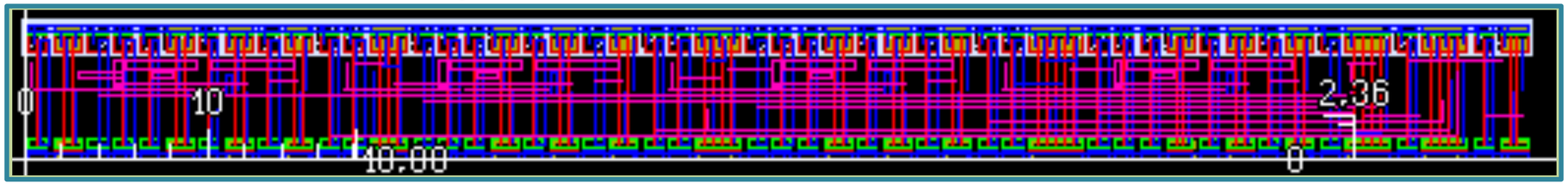


Figure 6



APPLICATIONS

- Comparators are used in central processing units (CPUs) and microcontrollers (MCUs).
- These are used in control applications in which the binary numbers representing physical variables such as temperature, position, etc. are compared with a reference value.
- Comparators are also used as process controllers and for Servo motor control.
- Used in password verification and biometric applications.

REFERENCES

- Tripathy, S. (2015). Low Power, high speed 8-bit magnitude comparator in 45NM technology for Signal Processing Application. *Indian Journal of Science and Technology*, *8*(1), 1–10. https://doi.org/10.17485/ijst/2016/v9i13/78981
- Magnitude comparator in digital logic. GeeksforGeeks. (2022, June 15). Retrieved December 1, 2022, from https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/

SOLUTION

From our proposed solutions, we found many inferences. The Dynamic Comparator excels at speed with minimum delay across the system, but struggles with area, pricing and design. Inversely, the sequential adds about 10% more delay but excels in minimum area with a better structure and less introduced components. In essence, the dynamic is more applicable in higher rated designs as the delay can be significant in multilevel systems. For more reduced designs, the sequential aims to be a better option.

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