VLSI 4-BIT FAST FULL ADDER

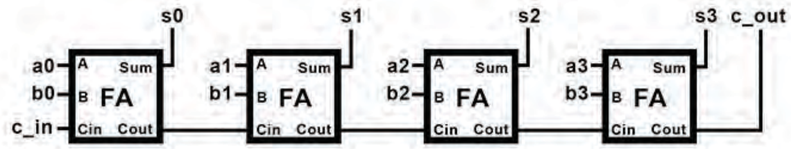
Chris Mlazgar

Faculty Mentor: Dr. Puteri Megat Hamari
ECET Department, Minnesota State University, Mankato

BACKGROUND

This project aims to develop a four bit VLSI fast full adder using the 90nm process. Goals for the project are to reduce layout area, latency, and power dissipation as much as possible by keeping capacitances low. The final design is composed of multiple tiers of sub-design work to achieve the intended function. The four bit full adder is capable of adding two four bit bytes together with support for a carry bit. Including the carry bit allows this design to produce five bit values with a decimal range from zero to 31. The general schematic for the four bit full adder can be seen in Figure 1 below.

FIGURE 1: FOUR BIT FULL ADDER



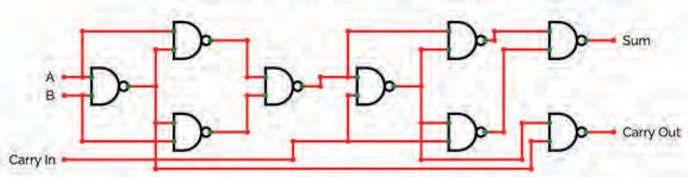
PROPOSED SOLUTION

The proposed solution to this project centered around developing design sub-blocks that can be used successively during the three design phases. The building block for the entire design is the two-input NAND gate. All of the logic used to design the four bit full adder would be NAND logic. The NAND sub-block was then used to develop the single bit full adder. Using a truth table for a full adder I developed a logic circuit using AND and OR. This circuit was then simplified and translated to NAND logic. The truth table and NAND circuit can be seen in Figure 2 and Figure 3 respectfully.

FIGURE 2: FULL ADDER TRUTH TABLE

Input			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FIGURE 3: FULL ADDER NAND LOGIC

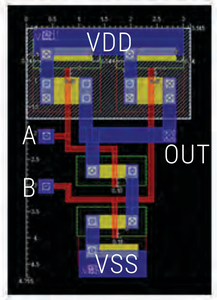


SYSTEM DESIGN

TWO INPUT NAND BLOCK

The project design is entirely comprised of two input NAND gates to reduce complexity and MOSFET counts. With that in mind I first set out to design a two input NAND gate that occupies as little area as possible. I ended up with a NAND gate that occupies a total area of 14.9μm^2. The gate contains two PMOS and two NMOS transistors with widths of 0.5μm and 0.25μm respectfully and both having a length of 1μm. This logic gate design results in a capacitance of 3aF or 3E10-18 farads. The layout of this NAND gate can be seen in Figure 4.

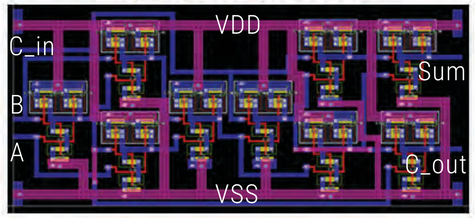
FIGURE 4: NAND LAYOUT



FULL ADDER BLOCK

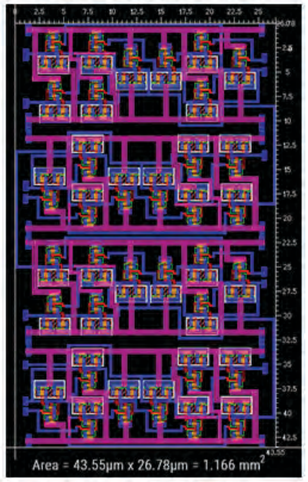
Using nine two input NAND blocks from Figure 4 I assembled a full adder referencing the logic diagram in Figure 3. I was careful to isolate inputs to the left side, outputs to the right, and power rails on top and bottom. This was done to make the final assembly as simple as possible. This full adder contains 36 MOSFETs which results in a total capacitance of 27aF or 27E10-18 farads. The layout occupies 388.75μm^2.

FIGURE 5: FULL ADDER LAYOUT



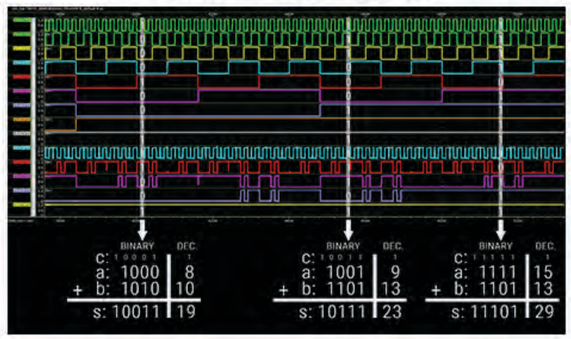
FOUR BIT FULL ADDER

FIGURE 6: FOUR BIT FA LAYOUT



The four bit full adder uses four vertically stacked full adder blocks from Figure 5 in a successive manner described by the image in Figure 1. In order to connect the VDD and VSS rails together each successive adder is rotated 90°. This also has the benefit of placing the inputs of the next adder near the ouputs of the previous adder reducing interconnect lengths. In simulations the adder was fed signals ranging from 1GHz to 3.9MHz which cycled through every input permutation. Figure 7 shows the waveforms from these tests as well as describes the arithmetic being performed. Total path delays for this adder were measured at 215ps when evaluated in a worst case scenario. Output signal rise times ranged from 18.5ps to 23.1ps with signal fall times ranging from 15.4ps to 26.4ps. The total capacitance calcualted for the final design came to 108aF or 108E10-18 farads. Using this value I calculated the total dynamic power dissipation generated by the design during operation to be 155.52nW. The final adder layout measures 43.55μm in height by 26.78μm in width resulting in a total area of 1.66 square mm. Comparing this design to other VLSI adders reveals that it dissipates more power but has a smaller total path delay. Results from (Wei) measured a path delay of around 650ps and power dissipation published by (Loo) were on the order of picowatts. Overall this design achieved correct function of a four bit fast full adder and I was satisfied with the results.

FIGURE 7: FULL ADDER SIMULATION



FUTURE DIRECTION

- More efficient area usage in the full adder sub-block
- Additional considerations for dynamic power dissipation
- Inclusion of look-ahead carry for fast carry bit calculation

ACKNOWLEDGEMENTS

Thank you to Dr. Hamari and the ECET department.

REFERENCES

Loo, Edward KW. "Low-voltage single-phase clocked quasi-adiabatic pass-gate logic family for low-power submicron VLSI CMOS applications."

Wei, Lan. "Implementation of Pipelined Bit-parallel Adders"

CONTACT INFORMATION

You can contact this team at CHRISTOPHER.MLAZGAR@MNSU.EDU with any questions or comments about the project.